a second cascode transistor having a base terminal coupled to the base terminal of the first cascode transistor, an emitter terminal coupled to a first terminal of a second inductor and to an emitter terminal of a first npn transistor and a collector terminal coupled to the first differentially coupled npn transistor pair,

a second capacitor, having a first terminal coupled to the emitter terminal of the second cascode transistor and a second terminal coupled to a second terminal of the first capacitor, the base terminal of the first cascode transistor and to the base terminal of the second cascode transistor,

a third capacitor, having a first terminal coupled to the emitter terminal of the first cascode transistor and a second terminal coupled to the second terminal of the second capacitor,

a second biasing resistor having a first terminal coupled to the first terminal of the second capacitor and a second terminal coupled to a second bias voltage.

(AMENDED)

14. A quadrature mixer circuit for generating a quadrature IF output responsive to an RF input and a quadrature pair of LO drive signals, comprising:

a mixer core having a first doubly balanced mixer including a first differentially coupled npn transistor pair and a second differentially coupled npn transistor pair and having a second doubly balanced mixer including a third differentially coupled npn transistor pair and a fourth differentially coupled npn transistor pair; the mixer core coupled to receive a quadrature LO drive signal, the quadrature LO drive signal having a plurality of harmonics;

a low noise RF input circuit coupled to the mixer core through a folded cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the folded cascode circuit further isolates the RF input circuit from the quadrature LO drive signal and the plurality of harmonics,

a first cascode capacitor, a first terminal of the first cascode capacitor coupled to the emitter terminal of a first cascode transistor and a second node of the first cascode capacitor coupled to the base terminals of the first cascode transistor and a second cascode transistor,

a second cascode capacitor, a first terminal of the second cascode capacitor coupled to the base terminals of the first cascode transistor and the second cascode transistor and the second node of the second cascode capacitor coupled to the emitter terminal of the second cascode transistor.